**Lab report no 5**



**Fall 2022**

**CSE-308L Digital Systems Design Lab**

**Submitted By**

**Names Registration No**

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Section: **A**

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**Lab task (7 segment counter): -**

module clk\_div(clk100MHz,clk1Hz,rst);

input clk100MHz;

input rst;

output reg clk1Hz;

integer count;

always @(posedge clk100MHz)

if(rst)

begin

count=0;

clk1Hz=0;

end

else

begin

count=count+1;

if(count==1000000)

begin

clk1Hz=~clk1Hz;

count = 0;

end

end

endmodule

module counter(clk100MHz, reset, count);

input clk100MHz, reset;

output [7:0] count;

reg [7:0] count;

wire clk1Hz;

clk\_div div(clk100MHz,clk1Hz,reset);

always @( posedge clk1Hz)

if(reset)

count <= 8'b10000000;

else

begin

count <= count << 1; //Shift Left (Fill with Zero)

count[0] <= count[7];

end

endmodule

# PlanAhead Generated physical constraints

NET "count[7]" LOC = P15;

NET "count[6]" LOC = P16;

NET "count[5]" LOC = N15;

NET "count[4]" LOC = N16;

NET "count[3]" LOC = U17;

NET "count[2]" LOC = U18;

NET "count[1]" LOC = T17;

NET "count[0]" LOC = T18;

NET "clk100MHz" LOC = V10;

NET "reset" LOC = F17;

# PlanAhead Generated IO constraints

NET "clk100MHz" PULLUP;

NET "reset" PULLUP;

**Ports outputs: -**

